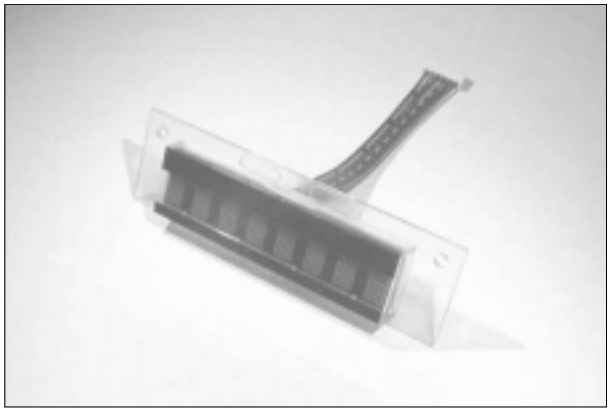
OSRAM

YELLOW SCF5781
HIGH EFFICIENCY RED SCF5782
GREEN SCF5783
HIGH EFFICIENCY GREEN SCF5784
ORANGE SCF5785

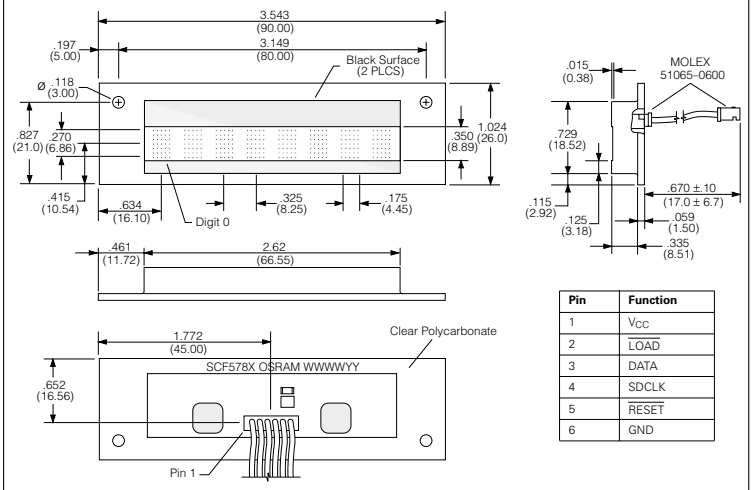
0.270" 8-Character 5x7 Dot Matrix Serial Input Dot Addressable Intelligent Display® Devices



FEATURES

- **Eight 0.270" (6.85 mm) 5x7 Dot Matrix Characters in Yellow, High Efficiency Red, Green, High Efficiency Green, Orange**
- **Optimum Display Surface Efficiency (display area to package ratio)**
- **High Speed Data Input Rate: 5.0 MHz**
- **ROMless Serial Input, Dot Addressable Display Ideal for User Defined Characters**
- **Built-in Decoders, Multiplexers and LED Drivers**
- **Readable from 8 to 10 Feet (2.5 to 3.0 meters)**
- **Attributes:**
  - **280 Bit RAM for User Defined Characters**
  - **16 Dimming Levels**
  - **Power Down Mode (<250 µW)**
  - **Hardware/Software Clear Functions**
  - **Internal Clock**
  - **3.3 V Capability**

Dimensions in Inches (mm)



Pin	Function
1	V_{CC}
2	$\overline{LOAD}$
3	DATA
4	SDCLK
5	$\overline{RESET}$
6	GND

Tolerance: x.xx ±.005 (x.xx ±.13)

DESCRIPTION

The SCF578X is a eight digit, dot addressable 5x7 dot matrix, serial input, alphanumeric Intelligent Display device. The digits are packaged in a rugged, high quality, optically transparent, plastic package.

Electrical connection is handled with a supplied 6 wire connector cable.

The on-board CMOS has a 280 bit RAM, one bit associated with one LED, each to generate User Defined Characters. In Power Down Mode, quiescent current is <50 µA.

Data is transferred into the display through the Serial Data Input (DATA), clocked by the Serial Data Clock (SDCLK), and enabled by the Load Input (LOAD).

Maximum Ratings

DC Supply Voltage ..... –0.5 to +7.0 Vdc
Input Voltage Levels Relative
to Ground ..... –0.5 to V_{CC} +0.5 Vdc
Operating Temperature ..... –40°C to +70°C
Storage Temperature ..... –40°C to +85°C
Relative Humidity at 85°C 85%
Maximum Number of LEDs on at 100% Brightness 160
Maximum Power Dissipation at 70°C ..... 1.65 W
ESD (100 pF, 1.5 kΩ) ..... 2.0 kV

Figure 1. Timing diagram—data write cycle

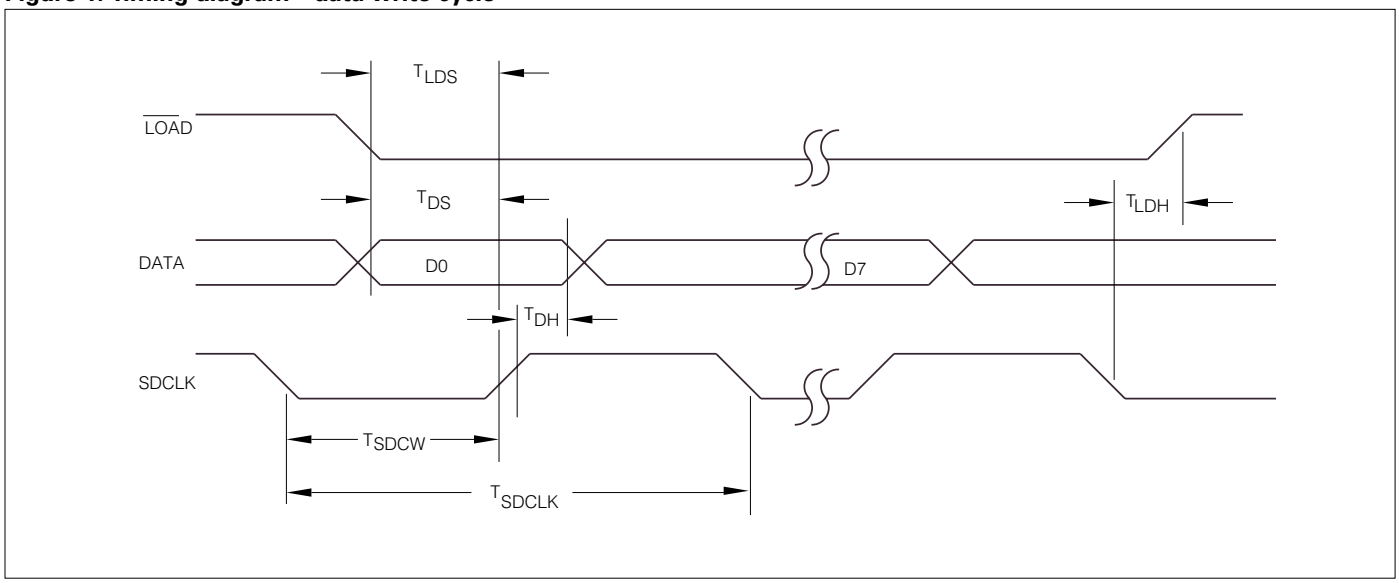
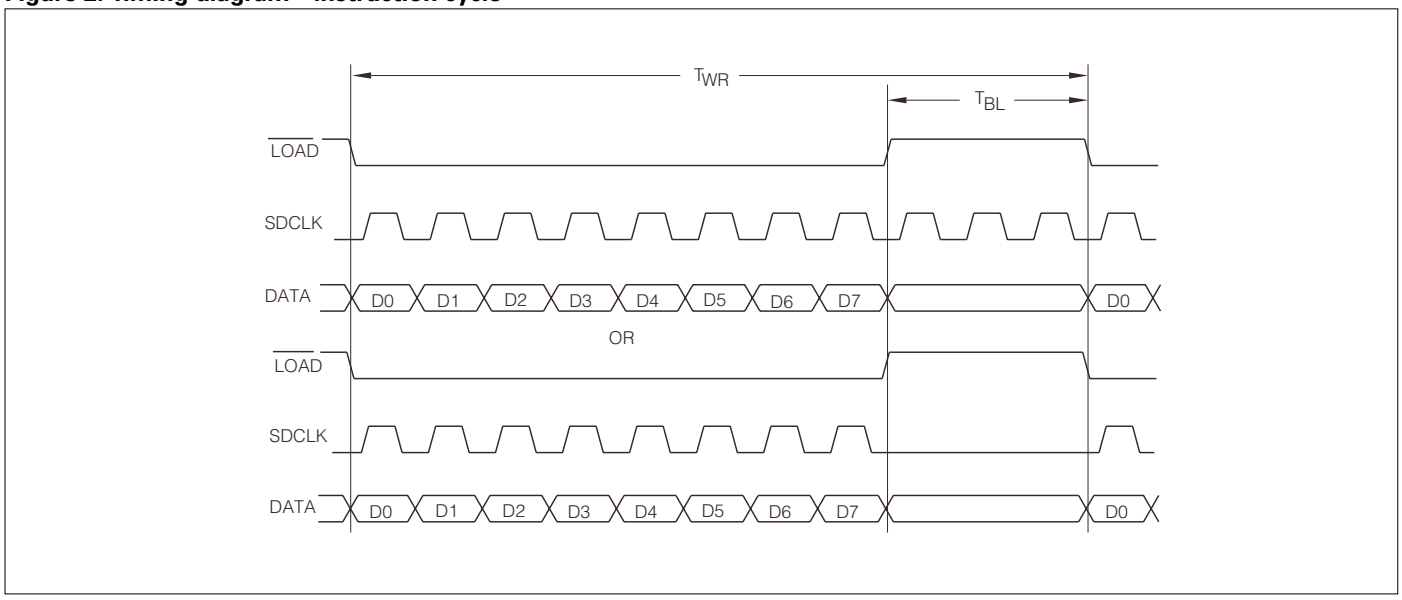


Figure 2. Timing diagram—instruction cycle



Optical Characteristics T_A=25°C
(V_{CC}=5.0 V at 100% brightness level)

Yellow SCF5781

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	60	200	µcd/dot
Peak Wavelength	λ_{peak}	—	583	nm
Dominant Wavelength	λ_{dom}	—	585	nm

High Efficiency Red SCF5782

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	60	200	µcd/dot
Peak Wavelength	λ_{peak}	—	630	nm
Dominant Wavelength	λ_{dom}	—	620	nm

Green SCF5783

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	60	200	µcd/dot
Peak Wavelength	λ_{peak}	—	565	nm
Dominant Wavelength	λ_{dom}	—	578	nm

High Efficiency Green SCF5784

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	80	250	µcd/dot
Peak Wavelength	λ_{peak}	—	568	nm
Dominant Wavelength	λ_{dom}	—	574	nm

Orange SCF5785

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	60	200	µcd/dot
Peak Wavelength	λ_{peak}	—	605	nm
Dominant Wavelength	λ_{dom}	—	610	nm

Notes:

1. Dot to dot intensity matching at 100% brightness is 1.8:1.
2. Displays within a given intensity category have an intensity matching of 1.5:1 (max.)

Switching specifications
(over operating temperature range and V_{CC}=4.5 V to 5.5 V)

Symbol	Description	Min.	Units
T_{RC}	Reset Active Time	600	ns
T_{LDS}	Load Setup Time	50	ns
T_{DS}	Data Setup Time	50	ns
T_{SDCLK}	Clock Period	200	ns
T_{SDCW}	Clock Width	70	ns
T_{LDH}	Load Hold Time	0	ns
T_{DH}	Data Hold Time	25	ns
T_{WR}	Total Write Time	2.25	µs
T_{BL}	Time Between Loads	600	ns

Note:

T_{SDCW} is the minimum time the SDCLK may be low or high.
The SDCLK period must be a minimum of 200 ns.

Electrical characteristics (over operating temperature)

Parameter	Min.	Typ.	Max.	Units	Conditions
V_{CC}	4.5	5.0	5.5	V	—
I_{CC} (PWR DWN)(1)	—	—	50	µA	V_{CC}=5.0 V, all inputs=0 V or V_{CC}
I_{CC} 4 digits(2) 20 dots/character	—	240	300	mA	V_{CC}=5.0 V, "#" displayed in all 8 digits at 100% brightness at 25°C
I_{IL} Input current	—	—	–10	µA	V_{CC}=5.0 V, V_{IN}=0 (all inputs)
I_{IH} Input current	—	—	10	µA	V_{CC}=V_{IN}=5.0 V (all inputs)
V_{IH}	3.5	—	—	V	V_{CC}=4.5 V to 5.5 V
V_{IL}	—	—	1.5	V	V_{CC}=4.5 V to 5.5 V
$\theta_{JC\text{-}pin}$	—	—	32	°C/W	—
FM, Digit	375	768	1086	Hz	—

Notes:

(1) Unused inputs must be tied high.
(2) Peak current $^5/_3$ x I_{CC}.

Input Circuits

Figure 3 shows the input resistor/diode networks used for ESD protection and to eliminate substrate latch-up caused by input voltage over/under shoot.

Figure 3. Inputs

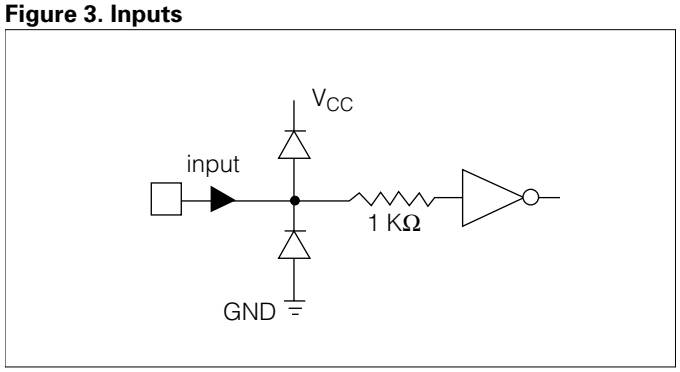


Figure 4. Dot matrix format

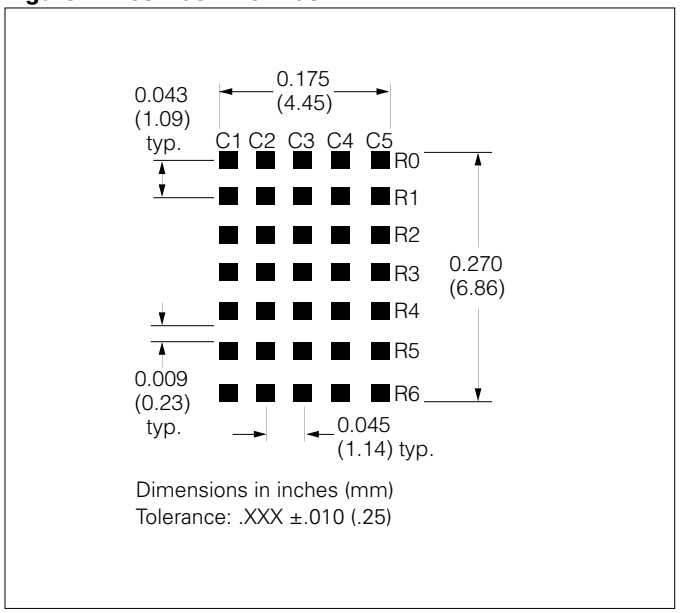
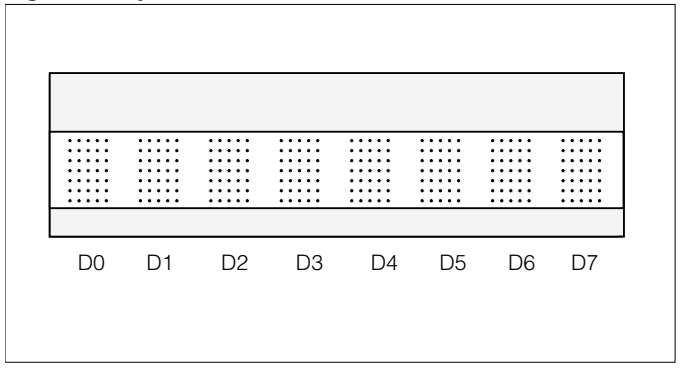


Figure 5. Top View



Pin definitions

Pin	Function	Definitions
1	V_{CC}	Logic supply
2	$\overline{LOAD}$	Low input enables data clocking into a serial shift register. When load goes high, the content of the shift register are decoded.
3	DATA	Serial data input
4	SDCLK	For loading data into the 8-bit serial data register
5	$\overline{RESET}$	Asynchronous input, when low clears the multiplex counter, address register, control word register, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.
6	GND	Supply ground

Display column and row format

	C0	C1	C2	C3	C4
Row 0	1	1	1	1	1
Row 1	0	0	1	0	0
Row 2	0	0	1	0	0
Row 3	0	0	1	0	0
Row 4	0	0	1	0	0
Row 5	0	0	1	0	0
Row 6	0	0	1	0	0

1=Display dot "On"
0=Display dot "Off'

Column data ranges

Row 0	00H to 1FH
Row 1	00H to LFH
Row 2	00H to LFH
Row 3	00H to LFH
Row 4	00H to LFH
Row 5	00H to LFH
Row 6	00H to LFH

Figure 6. Block diagram

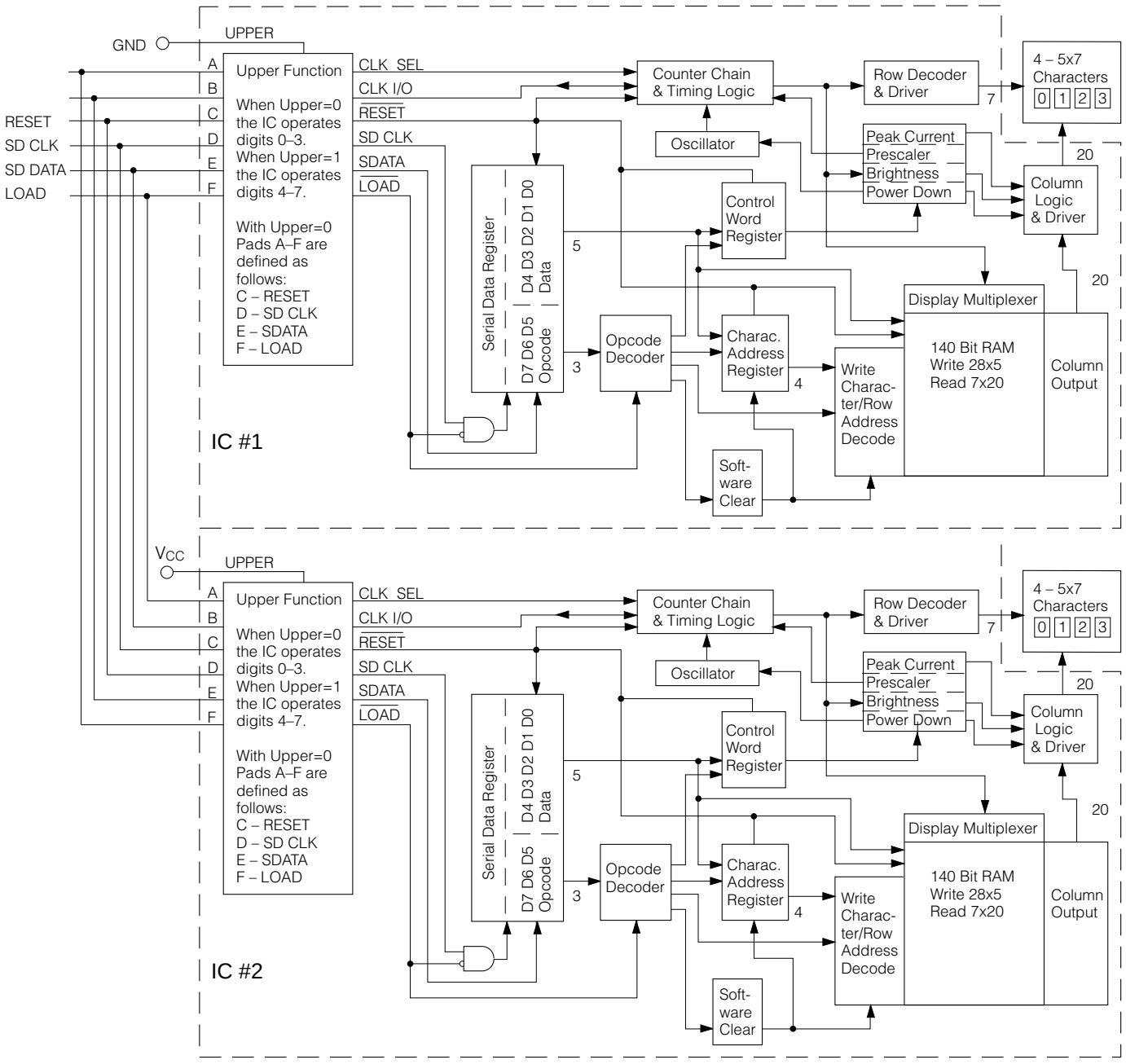
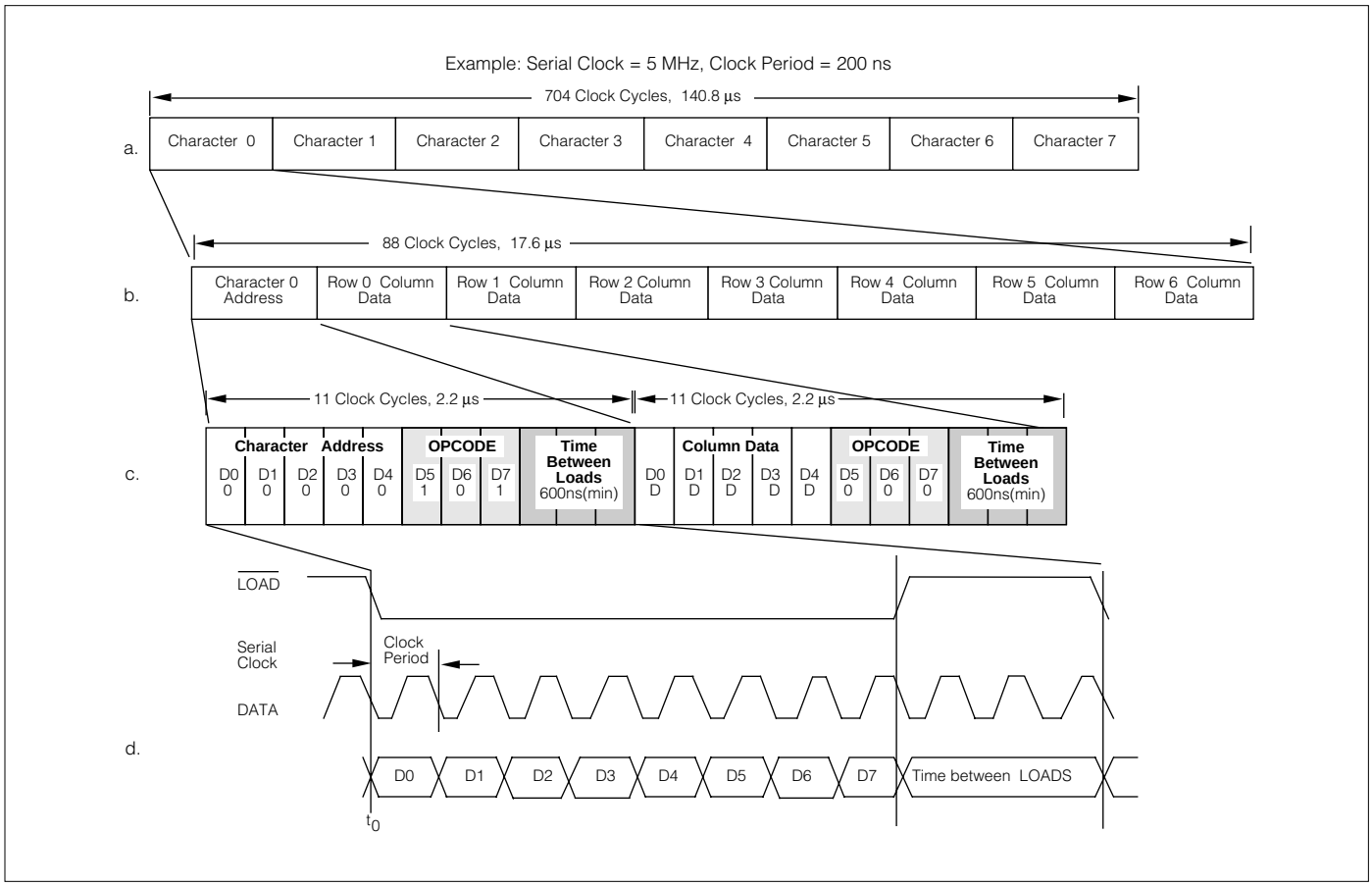


Figure 7. Loading serial character data



Operation of the SCF578X

The SCF578X display consists of two CMOS ICs containing control logic and drivers for four 5x7 characters. These components are assembled in a compact plastic package.

Individual LED dot addressability allows the user great freedom in creating special characters or mini-icons.

The CMOS compatible serial data interface provides a highly efficient interconnection between the display and the mother board. The SCF578X requires only three lines as compared to 14 for an equivalent four character parallel input part.

The on-board CMOS ICs are the electronic heart of the display. The ICs accepts decoded serial data, which is stored in the internal RAM. Asynchronously the RAM is read by the internal character multiplexer at a strobe rate that results in a flicker free display. Figure 5 shows the three functional areas of the ICs. These include: the input serial data register and control logic, 2 140 bits two port RAMs, and internal multiplexer/display drivers.

The following explains how to format the serial data to be loaded into the display. The user supplies a string of bit mapped decoded characters. The contents of this string is shown in Figure 7a. Figure 7b shows that each character consist of eight 8 bit words. The first word encodes the display character location and the succeeding seven bytes are row data. The row data represents the status (On, Off) of individual column LEDs. Figure 7c shows that each 8 bit word is formatted to represent Character Address, or Column Data.

Figure 7d shows the sequence for loading the bytes of data. Bringing the $\overline{\text{LOAD}}$ line low enables the serial register to accept data. The shift action occurs on the low to high transition of the serial data clock (SDCLK). The least significant bit (D0) is loaded first. After eight clock pulses the $\overline{\text{LOAD}}$ line is brought high. With this transition the OPCODE is decoded. The decoded OPCODE directs D4–D0 to be latched in the Character Address register, stored in the RAM as Column data, or latched in the Control Word register. The control IC requires a minimum 600 ns delay between successive byte loads. As indicated in Figure 7a, a total of 704 bits of data are required to load all 8 characters into the display.

Table 1 shows the Row Address for the example character "D." Column data is written and read asynchronously from the RAM. Once loaded the internal oscillator and character multiplexer reads the data from the RAM. These characters are row strobed with column data as shown in Figures 8 and 9. The character strobe rate is determined by the internal MUX Clock and the IC's ÷ 320 counter.

Table 1. Character "D"

	Op code D7	D6	D5	Column Data D4 C0	D3 C1	D2 C2	D1 C3	D0 C4	Hex
Row 0	0	0	0	1	1	1	1	0	1E
Row 1	0	0	0	1	0	0	0	1	11
Row 2	0	0	0	1	0	0	0	1	11
Row 3	0	0	0	1	0	0	0	1	11
Row 4	0	0	0	1	0	0	0	1	11
Row 5	0	0	0	1	0	0	0	1	11
Row 6	0	0	0	1	1	1	1	0	1E

Figure 8. Row and column locations for a character "D"

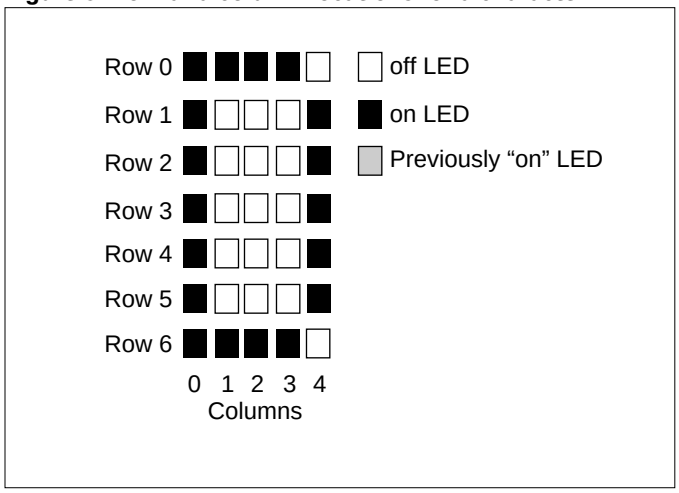
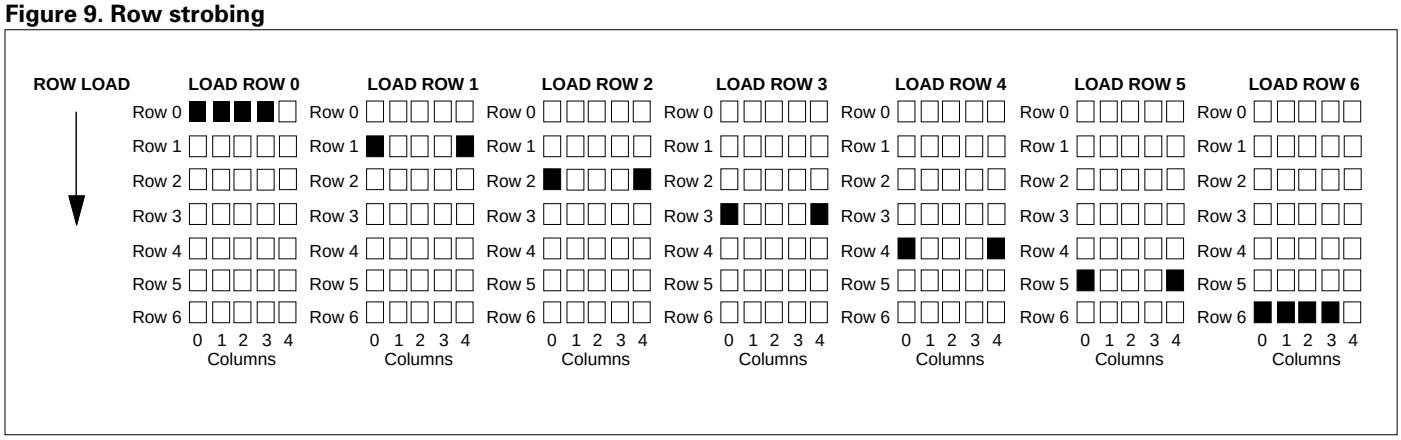


Figure 9. Row strobing



Basic Intruction Set

Instruction	Opcode	Address/Data	Comments
LCD	000	D4 D3 D2 D1 D0	Load Column Data
LDA	101	X X A2 A1 A0	Load Digit Address
SCL	110	PS B3 B2 B1 B0	Software Clear
LCWD	111	PS B3 B2 B1 B0	Load Control Word Data

The OPCODEs and Control Words for the Character Address and Loading Column Data are shown in Tables 2 and 3.

Table 2. Load character address

Op code D7	D6	D5	Character Address D4	D3	D2	D1	D0	Hex	Operation Load
1	0	1	0	0	0	0	0	A0	Character 0
1	0	1	0	0	0	0	1	A1	Character 1
1	0	1	0	0	0	1	0	A2	Character 2
1	0	1	0	0	0	1	1	A3	Character 3

Table 3. Load column data

Op code D7	D6	D5	Column Data D4	D3	D2	D1	D0	Operation Load
0	0	0	C0	C1	C2	C3	C4	Row 0
0	0	0	C0	C1	C2	C3	C4	Row 1
0	0	0	C0	C1	C2	C3	C4	Row 2
0	0	0	C0	C1	C2	C3	C4	Row 3
0	0	0	C0	C1	C2	C3	C4	Row 4
0	0	0	C0	C1	C2	C3	C4	Row 5
0	0	0	C0	C1	C2	C3	C4	Row 6

The Software Clear ($C0_{HEX}$), given in Table 4, clears the Address Register and the RAM. The display is blanked and the Character Address Register will be set to Character 0. The internal counter and the Control Word Register are unaffected. The Software Clear will remain active until the next data input cycle is initiated.

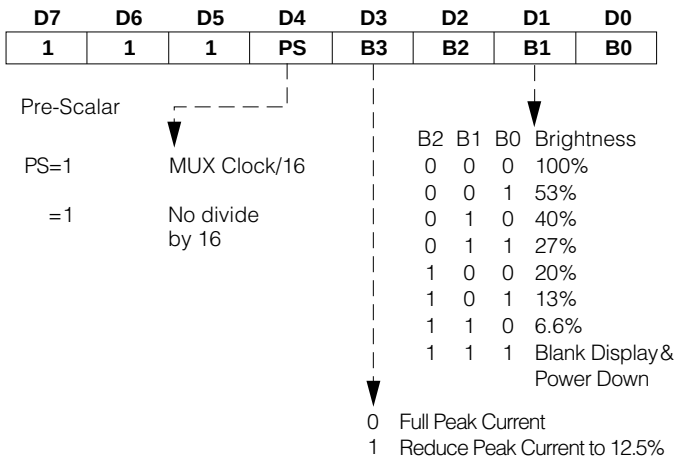
Table 4. Software clear

Op code D7	D6	Control Word D5	D4	D3	D2	D1	D0	Hex	Operation
1	1	0	0	0	0	0	0	C0	CLEAR

Control Word Register:

The Control Word is a 5 bit write only register which controls the display attributes. Below are the truth tables which defines each bit in the Control word Register and a description of their functions.

Control Word Format



The user can activate Control functions. These are: LED Brightness Level, IC Power Down and Prescaler. OPCODEs and six bit words are used to initiate these functions.

The SCF578X offers a unique Display Power Down feature which reduces I_{CC} to less than 50 µA. When EF_{HEX} is loaded the display is set to 0% brightness. When in the Power Down mode data may still be written into the RAM. The display is reactivated by loading a new brightness Level Control Word into the display.

Table 5. Power down

Op code D7	D6	Control Word D5	D4	D3	D2	D1	D0	Hex	Operation Level
1	1	1	0	1	1	1	1	EF	0% brightness

Prescaler

The prescaler is provided for use with a high speed external clock. This part uses an internal clock only so the built-in prescaler should not be used. In the control word format always set data bit D4 high (D4=1). If D4 is low the internal clock is divided by 16 (not recommended).

Note:

D4 is taken low to put the part in power down mode. See Table 5.

The user can slelct eight specific LED brightness levels (Table 6) by changing the peak current driving the LEDs. The peak current is varied by varying the ON time of the row drivers. Note that data line 3 is low (logic 0).

If dimming is required with finer control between 12.5% brightness and 0.0% brightness, data line 3 can be set high (logic 1). The 12.5% peak current is now the brightness reference (100%-E8) for further dimming and as shown in Table 7 eight levels of dimming are provided. For example the hex code EC in Table 7 will provide a brightness level 29% lower than the 12.5% brightness level.

Table 6. Display brightness

Op code		Control Word						Hex	Operation Level
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	1	0	0	0	0	0	E0	100%
1	1	1	0	0	0	0	1	E1	53%
1	1	1	0	0	0	1	0	E2	40%
1	1	1	0	0	0	1	1	E3	27%
1	1	1	0	0	1	0	0	E4	20%
1	1	1	0	0	1	0	1	E5	13%
1	1	1	0	0	1	1	0	E6	6.6%
1	1	1	0	0	1	1	1	E7	0.0%

Table 7. Display brightness

Op code		Control Word						Hex	Operation Level
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	1	0	1	0	0	0	E8	100%
1	1	1	0	1	0	0	1	E9	53%
1	1	1	0	1	0	1	0	EA	40%
1	1	1	0	1	0	1	1	EB	27%
1	1	1	0	1	1	0	0	EC	20%
1	1	1	0	1	1	0	1	ED	13%
1	1	1	0	1	1	1	0	EE	6.6%
1	1	1	0	1	1	1	1	EF	0.0%

The Software Clear ($C0_{HEX}$), given in Table 7, clears the Address Register and the RAM. The display is blanked and the Character Address Register will be set to Character 0. The internal counter and the Control Word Register are unaffected. The Software Clear will remain active until the next data input cycle is initiated.

Multiplexer and Display Driver

The eight characters are row multiplexed with RAM resident column data. The strobe rate is established by the internal MUX Clock rate. The MUX Clock frequency is divided by a 448 counter chain. This results in a typical strobe rate of 768 Hz.

An asynchronous hardware Reset is also provided. Bringing this pin low will clear the Character Address Register, Control Word Register, RAM, and blanks the display. This action leaves the display set at Character Address 0, and the Brightness Level set at 100%.

Electrical and Mechanical Considerations

Thermal Considerations

Optimum product performance can be had when the following electrical and mechanical recommendations are adopted. The SCF578X's ICs are constructed in a high speed CMOS process, consequently high speed noise on the SERIAL DATA, SERIAL DATA CLOCK, $\overline{LOAD}$ and $\overline{RESET}$ lines may cause incorrect data to be written into the serial shift register. Adhere to transmission line termination procedures when using fast line drivers and long cables (>10 cm).

Good ground and power supply decoupling will insure that I_{CC} (<400 mA peak) switching currents do not generate ground bounce. It is recommended that each display package use a 0.1 µF and 20 µF capacitor between V_{CC} and ground.

In applications where $\overline{RESET}$ will not be connected to the system's reset control, it is recommended that this pin be connected to the center node of a series 0.1, µF and 100 KΩ RC network. Thus upon initial power up the $\overline{RESET}$ will be held low for 10 ms allowing adequate time for the system power supply to stabilize.

ESD Protection

The input protection structure of the SCF578X provides significant protection against ESD damage. It is capable of withstanding discharges greater than 2 kV. Take all the standard precautions, normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. If these conditions are not, or cannot be met, keep the leads of the device shorted together or the parts in anti-static packaging.

Cleaning Procedures

The least offensive cleaning solution is hot D.I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Exercise care in choosing solvents as some may chemically attack the nylon package. For further information refer to Appnotes 18 and 19. See Appnote 19, Table 2, "Displays–Group 2".

Optical Considerations

The 0.270" high character of the SCF578X gives readability up to five feet. Proper filter selection enhances readability over this distance.

Using filters emphasizes the contrast ratio between a lit LED and the character background. This will increase the discrimination of different characters. The only limitation is cost. Take into consideration the ambient lighting environment for the best cost/benefit ratio for filters.

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are an inexpensive and effective way to strengthen contrast ratios. The SCF5782 is a high efficiency red display and should be used with long wavelength pass filter having a sharp cut-off in the 570 nm to 600 nm range. The SCF5784 is a high efficiency green display and should be used with long wavelength pass filter that peaks at 565 nm.

Additional contrast enhancement is gained by shading the displays. Plastic band-pass filters with built-in louvers offer the next step up in contrast improvement. Plastic filters can be improved further with anti-reflective coatings to reduce glare. The trade-off is fuzzy characters. Mounting the filters close to the display reduces this effect. Take care not to overheat the plastic filter by allowing for proper air flow.

Optimal filter enhancements are gained by using circular polarized, anti-reflective, band-pass filters. The circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1%.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homalite, Wilmington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY, Hoya Optics, Inc., Fremont, CA.

One last note on mounting filters: recessing displays and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several Bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E.-Atlas, Van Nuys, CA.

Data contents for the word "ABCD"

Step	D7	D6	D5	D4	D3	D2	D1	D0	Function
A	1	1	0	0	0	0	0	0	CLEAR
B (optional)	1	1	1	0	0	0	0	0	100% BRIGHTNESS
									DIGIT D0
1	1	0	1	0	0	0	0	0	SELECT
2	0	0	0	0	0	1	0	0	ROW 0 (A)
3	0	0	0	0	1	0	1	0	ROW 1 (A)
4	0	0	0	1	0	0	0	1	ROW 2 (A)
5	0	0	0	1	1	1	1	1	ROW 3 (A)
6	0	0	0	1	0	0	0	1	ROW 4 (A)
7	0	0	0	1	0	0	0	1	ROW 5 (A)
8	0	0	0	1	0	0	0	1	ROW 6 (A)
									DIGIT D1
9	1	0	1	0	0	0	0	1	SELECT
10	0	0	0	1	1	1	1	1	ROW 0 (B)
11	0	0	0	1	0	0	0	1	ROW 1 (B)
12	0	0	0	1	0	0	0	1	ROW 2 (B)
13	0	0	0	1	1	1	1	0	ROW 3 (B)
14	0	0	0	1	0	0	0	1	ROW 4 (B)
15	0	0	0	1	0	0	0	1	ROW 5 (B)
16	0	0	0	1	1	1	1	1	ROW 6 (B)
									DIGIT D2
17	1	0	1	0	0	0	1	0	SELECT
18	0	0	0	0	0	1	1	1	ROW 0 (C)
19	0	0	0	0	1	0	0	0	ROW 1 (C)
20	0	0	0	1	0	0	0	0	ROW 2 (C)
21	0	0	0	1	0	0	0	0	ROW 3 (C)
22	0	0	0	1	0	0	0	0	ROW 4 (C)
23	0	0	0	0	1	0	0	0	ROW 5 (C)
24	0	0	0	0	0	1	1	1	ROW 6 (C)
									DIGIT D3
25	1	0	1	0	0	0	1	1	SELECT
26	0	0	0	1	1	1	1	0	ROW 0 (D)
27	0	0	0	1	0	0	0	1	ROW 1 (D)
28	0	0	0	1	0	0	0	1	ROW 2 (D)
29	0	0	0	1	0	0	0	1	ROW 3 (D)
30	0	0	0	1	0	0	0	1	ROW 4 (D)
31	0	0	0	1	0	0	0	1	ROW 5 (D)
32	0	0	0	1	1	1	1	0	ROW 6 (D)

Power Up Sequence

Upon power up display will come on at random. Thus the display should be reset at power-up. The reset will set the Address Register to Digit 0, User RAM is set to 0 (display blank) the Control Word is set to 0 (100% brightness) and the internal counters are reset.

Loading Data into the Display

Use following procedure to load data into the display:

1. Power up the display.
2. Bring $\overline{RST}$ low (600 ns duration minimum) to clear the Multiplex Counter, Address Register, Control Word Register, User Ram and Data Register. The display will be blank. Display brightness is set to 100%.
3. If a different brightness is desired, load the proper brightness opcode into the Control Word Register.
4. Load the Digit Address into the display.
5. Load display row and column data for the selected digit.
6. Repeat steps 4 and 5 for all digits.

Operating Precautions

The CMOS device contains circuity to protect the input against damage due to high static voltage or electric fields. However, it is advised that normal precaution be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that all input voltages bi constrained to the range Gnd≤V≤Vcc/ VII, particularly during power conditions.

The recommended cleaning solutions for this product are found in Appnote 19, Display Group 1.
They are:
CFCs (ozone depleting substance): TF, TE, TMS
Non CFC: IPA
Semi-aqueous: Axarel 38, EC7R, Ionox LC, Ionox MC.

Molex cables and connector part numbers are:

Molex Cable P/N	053-0231
Molex Header P/N	053-1100

Microprocessor Interface

The microprocessor interface is through a serial port, SPI port or one of the eight data bits of an eight bit parallel port. The SDCLK, $\overline{\text{LOAD}}$ and $\overline{\text{RESET}}$ too are controlled from one of eight bit ports. See Figures 10, 11 and 12.

Note: All inputs require CMOS levels..

Figure 10. Display interface to Intel 8031 microprocessor
(using serial port in mode 0)

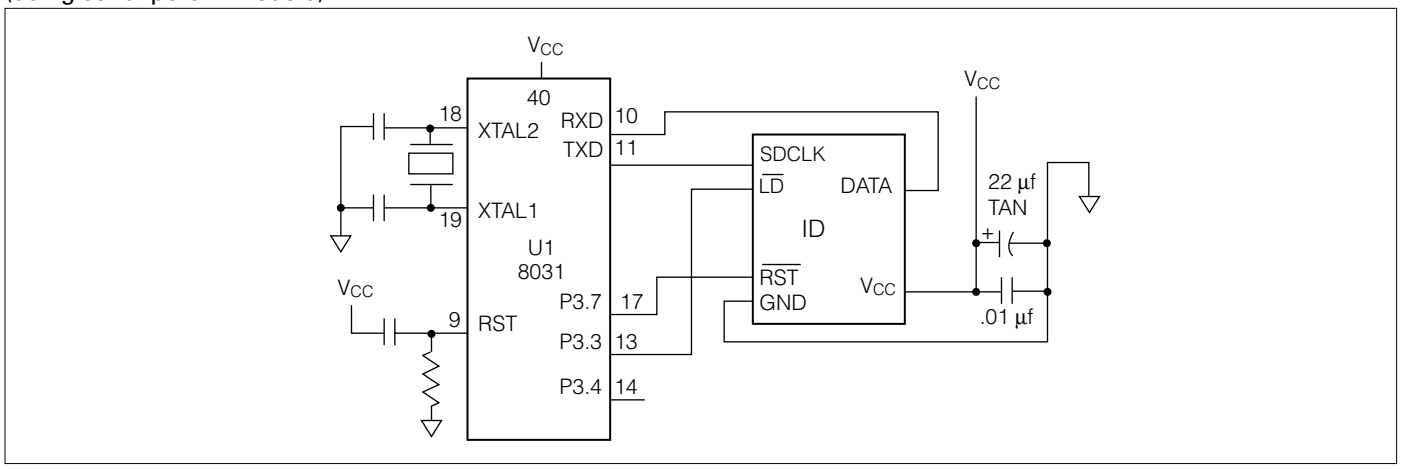


Figure 11. Display interface to Intel 8031 microprocessor
(using one bit of parallel port as serial port)

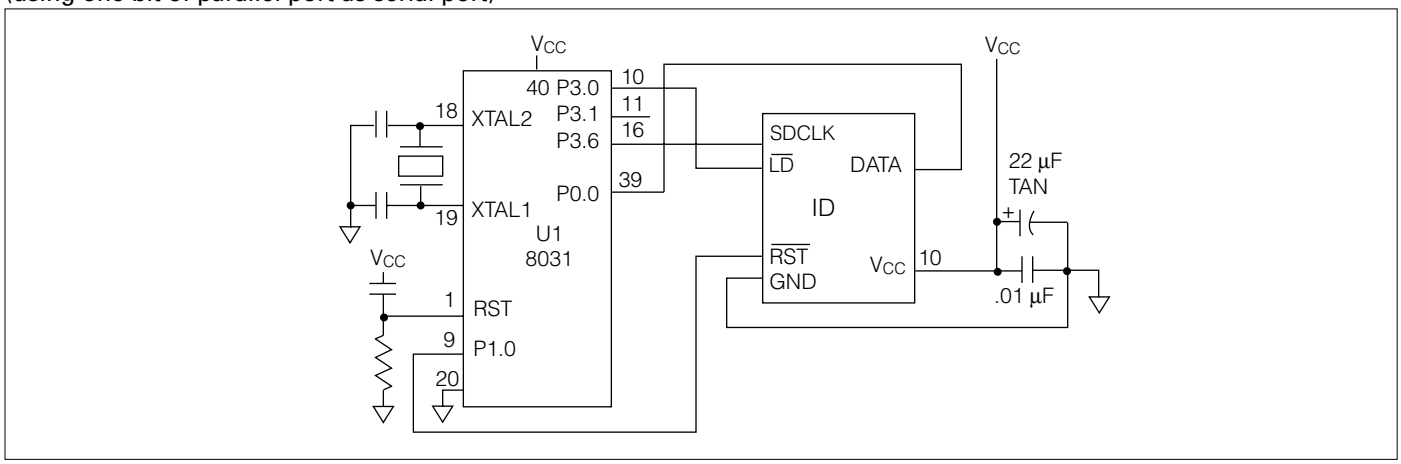


Figure 12. Display interface with Motorola 68HC05C4 microprocessor
(using SPI port)